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VLSI TOPICS

RESEARCH AND CONFERENCE ORIENTED TITLES

IEEE 2016

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VLSI – SIMULATION & HARDWARE DESIGN

DOMAIN	SINO	TOPIC	CODE
VLSI TOOL USED: XILINX / ALTERA	1	Total Jitter of Delay-Locked Loops Due to Four Main Jitter Sources	VL1601
	2	Multiple-parameter CMOS IC testing with increased sensitivity for I/sub DDQ/	VL1602
	3	A Single-Stage Low-Dropout Regulator With a Wide Dynamic Range for Generic Applications	VL1603
	4	A Capacitor-Less LDO With High-Frequency PSR Suitable for a Wide Range of On-Chip Capacitive Loads	VL1604
	5	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	VL1605
	6	Built-in Self-Calibration and Digital-Trim Technique for 14-Bit SAR ADCs achieving ±1 LSB INL	VL1606
	7	Minitaur, an Event-Driven FPGA-Based Spiking Network Accelerator	VL1607
	8	A Top–Down Design Methodology Encompassing Components Variations Due to Wide-Range Operation in Frequency Synthesizer PLLs	VL1608
	9	Design of Silicon Photonic Interconnect ICs in 65-nm CMOS Technology	VL1609
	10	Low-Power ECG-Based Processor for Predicting Ventricular Arrhythmia	VL1610
	11	A Systematic Design Methodology of Asynchronous SAR ADCs	VL1611
	12	Toward Solving Multichannel RF-SoC Integration Issues Through Digital Fractional Division	VL1612
	13	Optimized Built-In Self-Repair for Multiple Memories	VL1613
	14	Noise Modeling and Analysis of SAR ADCs	VL1614
	15	A Sub-mW, Ultra-Low-Voltage, Wideband Low-Noise Amplifier Design Technique	VL1615
	16	A Low-Power Class-AB Gm-Based Amplifier With Application to an 11-bit Pipelined ADC	VL1616
	17	High-Speed, Low-Power, and Highly Reliable Frequency Multiplier for DLL-Based Clock Generator	VL1617
	18	Design of a Low-Voltage Low-Dropout Regulator	VL1618
	19	Glitch Energy Reduction and SFDR Enhancement Techniques for Low-Power Binary-Weighted Current-Steering DAC	VL1619
	20	A Mismatch-Insensitive Skew Compensation Architecture for Clock Synchronization in 3-D ICs	VL1620
	21	A Programmable and Configurable Mixed-Mode FPAA SoC	VL1621
	22	Concept, Design, and Implementation of Reconfigurable CORDIC	VL1622

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VLSI – SIMULATION & HARDWARE DESIGN

SINO	TOPIC	CODE
23	5-bit 5-GS/s Non interleaved Time-Based ADC in 65-nm CMOS for Radio-Astronomy Applications	VL1623
24	Efficient Warranty-Aware Wear Leveling for Embedded Systems With PCM Main Memory	VL1624
25	Uniform Quantization Theory-Based Linearity Calibration for Split Capacitive DAC in an SAR ADC	VL1625

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